Lab 3 Verilog FIR Design Report

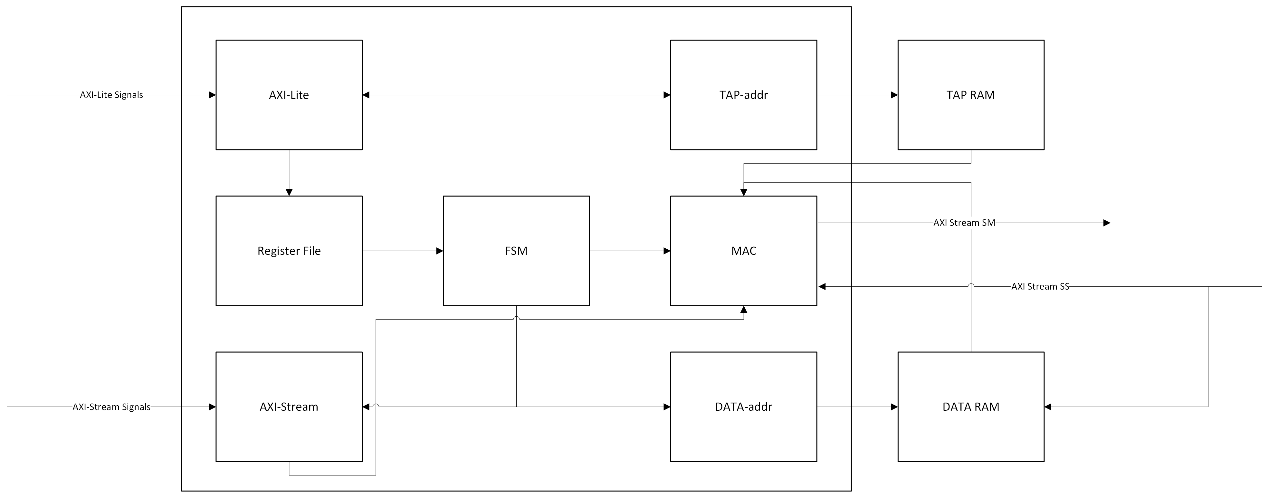
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**Block Diagram**



**Operation**

In this lab, we aim to construct a Finite Impulse Response (FIR) operation module with 11 coefficients to perform filtering. The module’s data must adhere to the AXI-Stream protocol.

**1. AXI-Lite Interface**

Configuration Management:

Handles writes for tap coefficients (awaddr ≥ 0x20) and control signals (ap\_start, data\_length at awaddr=0x00 and 0x10).

Reads status signals (ap\_done, ap\_idle) via araddr=0x00.

**2. Initialization Phase**

IDLE State:

Configuration register set to 32'h04.

Host writes tap coefficients to Tap\_RAM (addresses 0x20 to 0x48) and data\_length to awaddr=0x10.

Tap\_RAM Initialization: Coefficients stored sequentially at addresses 0, 4, 8, ..., 40.

**3. Transition to CAL State**

Start Signal:

Host sets ap\_start=1 (awaddr=0x00), transitioning to CAL state.

Data Loading:

AXI-Stream input ss\_tdata writes raw data into Data\_RAM using a sliding window address pattern (e.g., 0, 40, 36, ..., 4 for the first input).

**4. Address Generation Logic**

Tap\_RAM Access:

Coefficients read sequentially at 0, 4, 8, ..., 40 (11-tap cycle).

Data\_RAM Access:

Addresses follow a sliding window:

1st iteration: 0, 40, 36, ..., 4

2nd iteration: 4, 0, 40, ..., 8

Continues until the 11th iteration.

**5. Computation Phase**

MAC Unit Operation:

tap\_Do (coefficients) and data\_Do (input data) are multiplied and accumulated into FIR\_temp over 12 cycles (fir\_cycle\_cnt).

After 11 iterations, sm\_tvalid asserts to output the result sm\_tdata (Y).

**6. Completion and Output**

Data Length Tracking:

Internal counter fir\_data\_cnt tracks processed data blocks.

When fir\_data\_cnt == data\_length, ss\_tlast asserts, and the final result triggers sm\_tlast and ap\_done.

State Transition:

System enters DONE state after final computation, resetting to IDLE upon status read.

**7. Timing Optimization**

BRAM Latency Compensation:

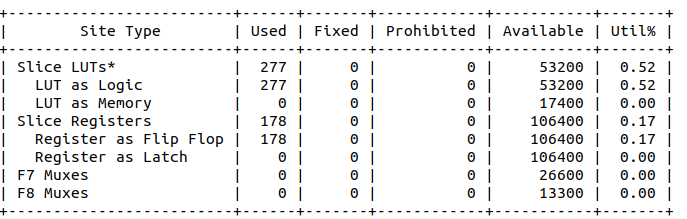
SS\_data (input) is delayed by 1 cycle via flip-flop (FF) to align with data\_Do availability.

Preloading First Tap:

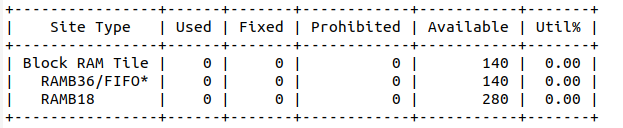
First coefficient is preloaded at CAL state entry to eliminate tap\_Do wait cycles.

**Resource Usage**

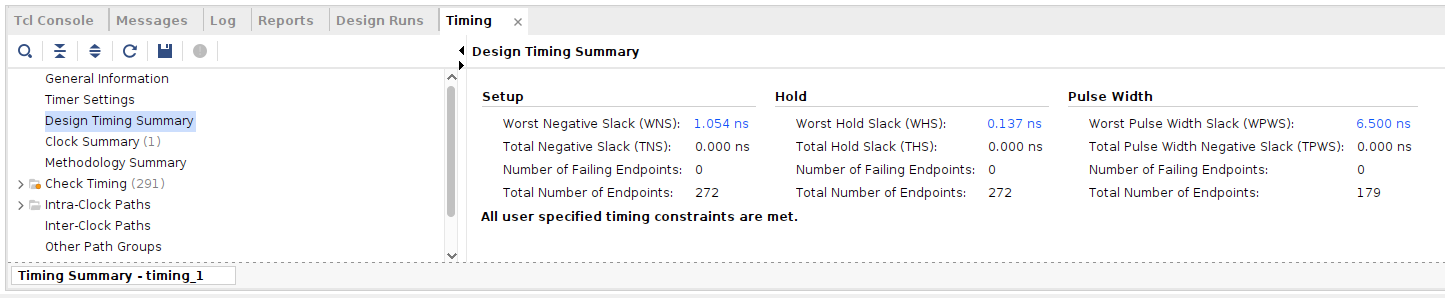
FF and LUT

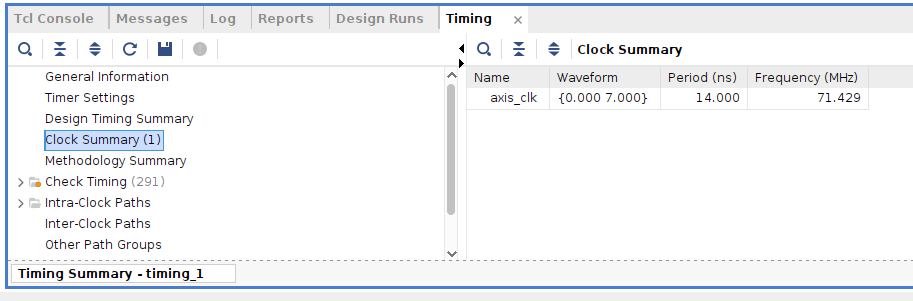


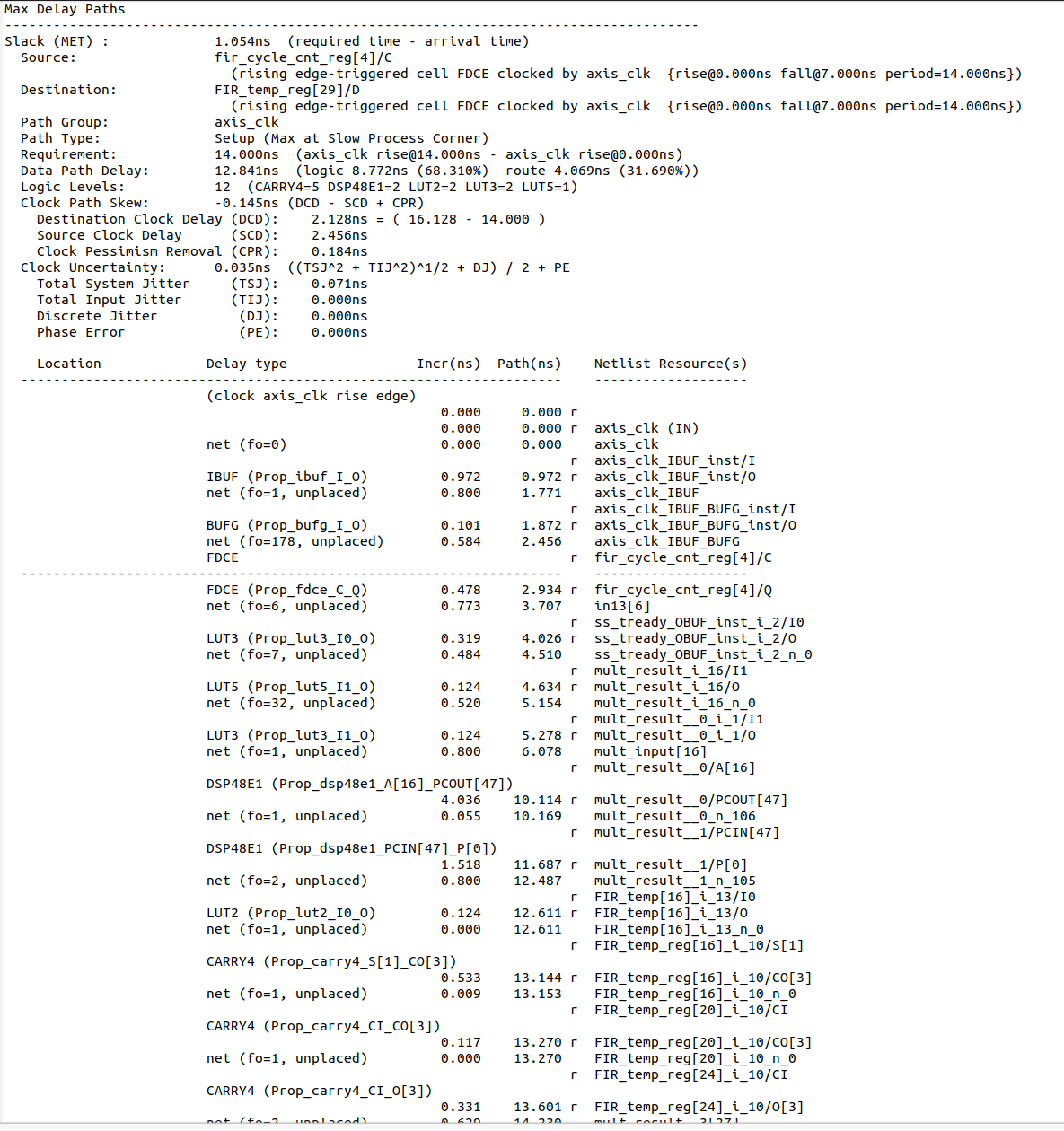
BRAM

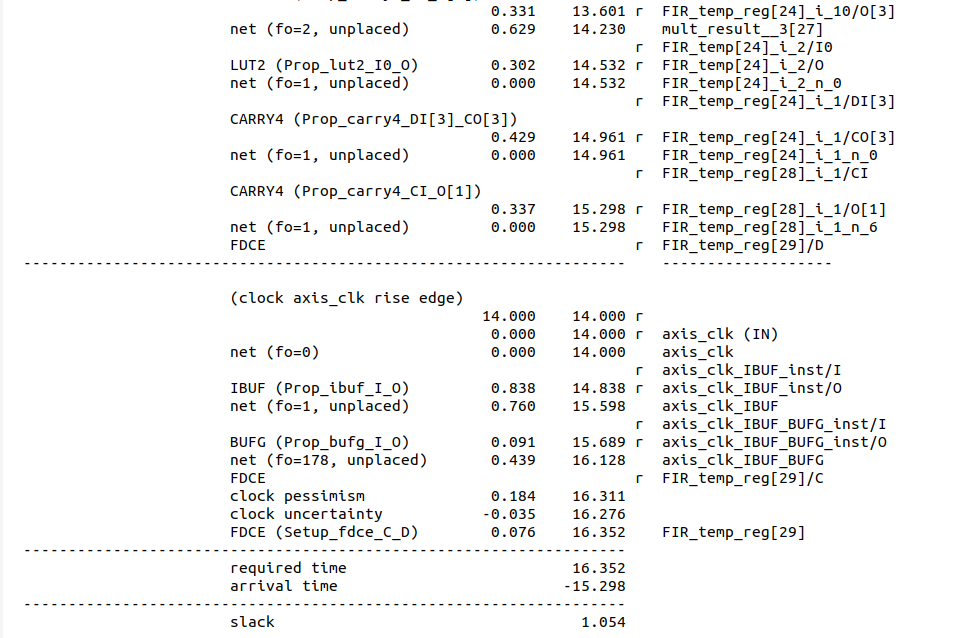


Timing Report



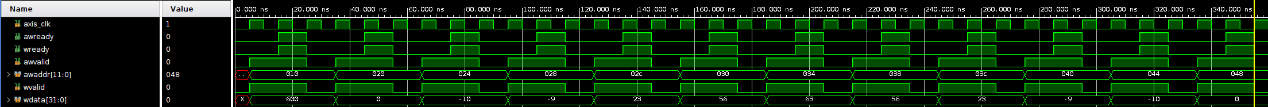




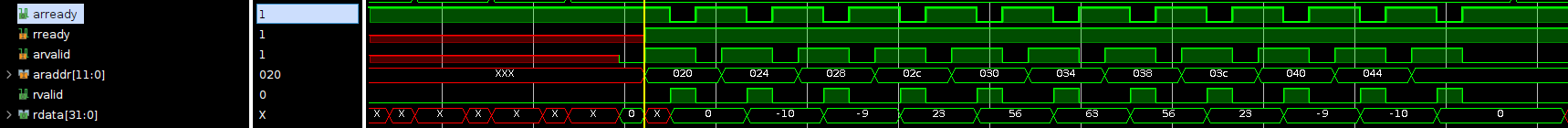


**Simulation waveform**

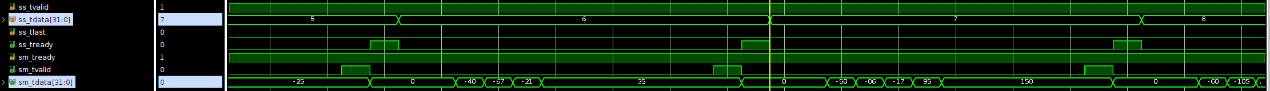
Coefficient program



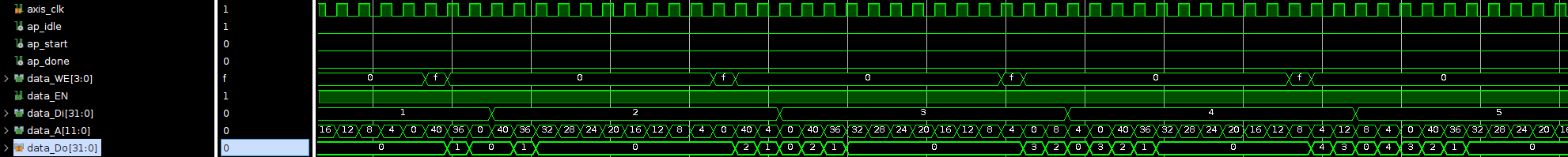
Read back

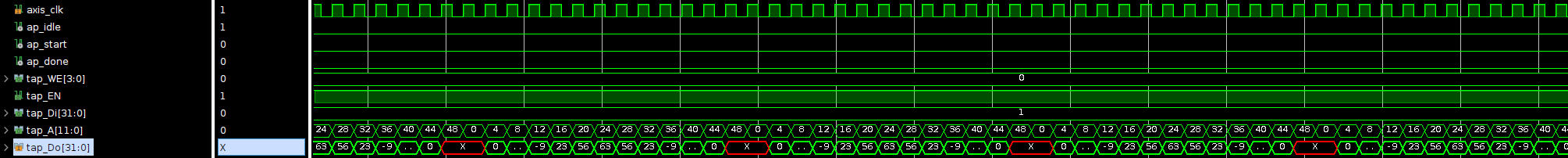


Data-in Stream-in && Data-out Stream-OUT

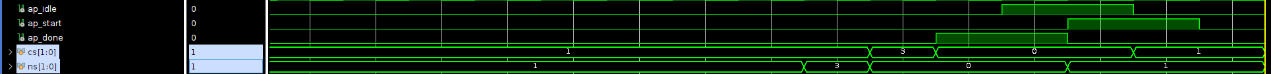


RAM access control





FSM



**Github:** https://github.com/TouHou-Yukari/EESM6000C-SoC-Laboratory